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10/525,141	02/16/2005	Adrianus Sempel	NL 020756	1775

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EXAMINER	
JOSEPH, DENNIS P	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,141	SEMPEL ET AL.	
	Examiner	Art Unit	
	DENNIS P. JOSEPH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,8-12 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,8-12 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to arguments filed in application No. 10/525,141 on August 6, 2009. Claims 1, 2, 4, 5, 8-12, 14-16 are pending and have been examined.

Claim Rejections – 35 USC § 103

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1, 2, 5, 8, 9 and 11, 12 and 14-16 are** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US 2002/0005696 A1), in view of Rai et al. (US 6,888,528 B2) and further in view of Tam (US 2003/0117082)

Yamazaki teaches in Claim 1:

A display device comprising at least one picture element and a display driver device

(Figure 23 shows EL element 703 with the corresponding circuitry. Please note that 703 is still an actual EL element itself and is set to the same value as the EL element, [0410].

Please note opposite/counter electrodes) comprising a driving transistor **(Figure 23 shows driving transistor 708 which is connected to the EL element)** to be connected in series with the picture element in a first current path **(Figure 23 shows transistor 708 to be in line with resistor 707 and EL element 703. Also, it is a design choice whether it is in series or parallel),**

the display driver comprising means for monitoring and controlling the current in said first current path **(Figure 23, [0401] disclose a current generator 704. Read the negative terminal of the amplifier as the first current path. Please note the interchangeability of voltage and current means)**, wherein the means for monitoring include an amplifier having a first input connected to the first current path **(Figure 23, amplifier 706 with the first input as noted above. Please note the output is to the driving transistor)**, a second input connected to a second current path **(Figure 23, read the positive terminal of the amplifier as the second current path)**

Yamazaki also does not explicitly teach wherein the output of the amplifier is "**directly** connected via a **first switch** to a controlling connection of the driving transistor."

The use of switches is well known in the art to control the on/off application of various components in the circuitry.

To emphasize, in the same field of endeavors, display system circuits, Rai discloses in Figure 15 of a switch 35, which is used to apply a clamp signal to alter the voltage level sent to the display.

This is located at the output of the amplifier 60 and is then directly connected to the transistor 320. This is part of the brightness adjustment circuit 32, which as seen from Figure 13 is connected to the LCD panel 100.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to integrate the switch as taught by Rai with Yamazaki's circuitry, with the motivation that the switch can be used to control the application of the clamp signal, which in turns can control the contrast ratio and the image brightness. This accounts for the amount of ambient light affecting the display and the proper signal can be sent. (Rai, Column 14, Lines 32-38)

Yamazaki and Rai also do not explicitly teach that the "second input is connected to a **second switch** for allowing a control charge on a capacitor connected to the second input to control the control amplifier for maintaining a current provided to the picture element during a hold period after selection of the picture element."

As for the second switch, in the same field on endeavor, display system circuits, Tam discloses in Figure 3 of transistor T_5 placed between the positive terminal and the capacitor. As for T_5, this transistor is used as a control switch to store the voltage of the capacitor (Tam, [0023]). This is akin to Applicant's Figure 5 with the positive terminal, switch and capacitor. The capacitor is used to hold and maintain the selected picture element data.

Therefore, it would be obvious to one of ordinary skill in the art, at the time of the invention, to integrate the switch as taught by Tam with Yamazaki's circuitry, as modified by Rai, with the motivation that is common to use such switches to control the on/off application of key components in the circuitry. Furthermore, the switch controls the application of the capacitor to control the application of the stored data to be displayed.

Yamazaki teaches in Claim 2:

The display device as claimed in claim 1 wherein operation the current in the first current path is controlled by a current simultaneously passing in the second current path. **(As disclosed in Figure 23, the current in the first path is attached to the transistor 708 which is affected by the current in second path, so there is a direct effect)**

Yamazaki teaches in Claim 5:

A display device as claimed in claim 1, wherein, in operation, the current in the first current path is controlled by a charge stored by means of a current having passed in the second current path. **([0416] discloses the embodiment can be combined with embodiments 1 through 12. Figure 3 discloses a capacitor as part of 525 which sends a signal to the amplifier 527. The path is to the positive terminal which is the second current path. [0249])**

Yamazaki teaches in Claim 8:

The display device as claimed in claim 1, wherein the picture element is a luminescent element and the first current determines a luminescence of the luminescent element. **(Figure 23**

shows EL element 703 (read as luminescent element) and the first current is connected to the transistor 708 which is therein connected to the element)

Yamazaki teaches in Claim 9:

A display driver device comprising:

a driving transistor for driving **(Figure 23, transistor 708)**, a picture element **(EL element 703. Please note that 703 is still an actual EL element itself and is set to the same value as the EL element, [0410]. Please note opposite/counter electrodes)**;

a control amplifier **(Figure 23, amplifier 706)**, a controlling connection of the driving transistor being coupled to an output of the control amplifier **(Figure 23 shows transistor 708 which receives the output of the amplifier 706)**, a first input of the control amplifier being coupled to the first current path **(Figure 23, [0401] disclose a current generator 704. Read the negative terminal of the amplifier as the first current path. Please note the interchangeability of current and voltage means)**, a second input of the control amplifier being connected to a second current path **(Figure 23, read the positive terminal of the amplifier as the second current path)**, and an output of the control amplifier being connected to a controlling connection of the driving transistor **(Figure 23, the output of the amplifier connects to the transistor 708)**

Yamazaki also does not explicitly teach wherein the output of the amplifier is "**directly** connected via a **first switch** to a controlling connection of the driving transistor."

The use of switches is well known in the art to control the on/off application of various components in the circuitry.

To emphasize, in the same field of endeavors, display system circuits, Rai discloses in Figure 15 of a switch 35, which is used to apply a clamp signal to alter the voltage level sent to the display. This is located at the output of the amplifier 60 and is then directly connected to the transistor 320. This is part of the brightness adjustment circuit 32, which as seen from Figure 13 is connected to the LCD panel 100.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to integrate the switch as taught by Rai with Yamazaki's circuitry, with the motivation that the switch can be used to control the application of the clamp signal, which in turns can control the contrast ratio and the image brightness. This accounts for the amount of ambient light affecting the display and the proper signal can be sent. (Rai, Column 14, Lines 32-38)

Yamazaki and Rai also do not explicitly teach that the "second input is connected to a **second switch** for allowing a control charge on a capacitor connected to the second input to control the control amplifier for maintaining a current provided to the picture element during a hold period after selection of the picture element."

As for the second switch, in the same field on endeavor, display system circuits, Tam discloses in Figure 3 of transistor T_5 placed between the positive terminal and the capacitor. As for T_5, this

transistor is used as a control switch to store the voltage of the capacitor (Tam, [0023]). This is akin to Applicant's Figure 5 with the positive terminal, switch and capacitor. The capacitor is used to hold and maintain the selected picture element data.

Therefore, it would be obvious to one of ordinary skill in the art, at the time of the invention, to integrate the switch as taught by Tam with Yamazaki's circuitry, as modified by Rai, with the motivation that is common to use such switches to control the on/off application of key components in the circuitry. Furthermore, the switch controls the application of the capacitor to control the application of the stored data to be displayed.

Yamazaki teach in Claim 11:

The display driver device as claimed in claim 9, wherein the second current path comprises a current source. **(Yamazaki further discloses in [0403], current generator 704. Please note the interchangeability of voltage and current means)**

Yamazaki teaches in Claim 12:

A display driver device comprising:

A driving transistor for driving a picture element via a first current path **(Figure 23 shows transistor 708 which connects to the EL element 703. Please note that 703 is still an actual EL element itself and is set to the same value as the EL element, [0410]. Please note opposite/counter electrodes)** wherein, in operation, the current in the first current path is controlled by a charge stored by means of a current having passed in a second circuitry part **(**

Figure 23 shows the current for the negative terminal (read as the first current path) which is impacted by the current flowing through the positive terminal (read as the second current path). Please note the interchangeability of current and voltage means); and

a control amplifier having an output coupled to the driving transistor **(Figure 23, amplifier 706 with an output coupled to transistor 708)**, a first input of the control amplifier being coupled to the first current path **(Figure 23, negative terminal as discussed above)**, and a second input of the control amplifier being connected to a second current path **(Figure 23, positive terminal as discussed above)**

Yamazaki also does not explicitly teach wherein the output of the amplifier is "**directly** connected via a **first switch** to a controlling connection of the driving transistor."

The use of switches is well known in the art to control the on/off application of various components in the circuitry.

To emphasize, in the same field of endeavors, display system circuits, Rai discloses in Figure 15 of a switch 35, which is used to apply a clamp signal to alter the voltage level sent to the display. This is located at the output of the amplifier 60 and is then directly connected to the transistor 320. This is part of the brightness adjustment circuit 32, which as seen from Figure 13 is connected to the LCD panel 100.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to integrate the switch as taught by Rai with Yamazaki's circuitry, with the motivation that the switch can be used to control the application of the clamp signal, which in turns can control the contrast ratio and the image brightness. This accounts for the amount of ambient light affecting the display and the proper signal can be sent. (Rai, Column 14, Lines 32-38)

Yamazaki and Rai also do not explicitly teach that the "second input is connected to a **second switch** for allowing a control charge on a capacitor connected to the second input to control the control amplifier for maintaining a current provided to the picture element during a hold period after selection of the picture element."

As for the second switch, in the same field on endeavor, display system circuits, Tam discloses in Figure 3 of transistor T_5 placed between the positive terminal and the capacitor. As for T_5, this transistor is used as a control switch to store the voltage of the capacitor (Tam, [0023]). This is akin to Applicant's Figure 5 with the positive terminal, switch and capacitor. The capacitor is used to hold and maintain the selected picture element data.

Therefore, it would be obvious to one of ordinary skill in the art, at the time of the invention, to integrate the switch as taught by Tam with Yamazaki's circuitry, as modified by Rai, with the motivation that is common to use such switches to control the on/off application of key components in the circuitry. Furthermore, the switch controls the application of the capacitor to control the application of the stored data to be displayed.

Yamazaki teaches in Claim 14:

The display driver device of claim 6, wherein the control charge is stored by means of a current having passed in the second current path. **([0416] discloses the embodiment can be combined with embodiments 1 through 12. Figure 3 discloses a capacitor as part of 525 which sends a signal to the amplifier 527. The path is to the positive terminal which is the second current path. [0249])**

Yamazaki teaches in Claim 15:

The display driver device of claim 1, wherein the first input is an inverting input and the second input is a non-inverting input. **(Figure 23 shows the first input to be inverting and the second to be non-inverting for the amplifier 706)**

Yamazaki teaches in Claim 16:

The display driver device of claim 9, wherein the first input is an inverting input and the second input is a non-inverting input. **(Figure 23 shows the first input to be inverting and the second to be non-inverting for the amplifier 706)**

4. **Claims 4 and 10** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US 2002/0005696 A1), Rai et al. (US 6,888,528 B2) and Tam (US 2003/0117082), as applied to claims 2 and 9 above, and further in view of Inoue (US 6,469,455 B1)

Yamazaki teach in Claim 4:

The display device as claimed in claim 2, wherein the driving transistor **(Figure 23, transistor 708)**, but

Yamazaki do not explicitly teach the driving transistor "is a field effect transistor, and the controlling connecting is a gate of the field effect transistor."

However, in the same field of endeavor, displays for luminescent devices, Inoue teaches "the current switch 3 and boosting switch 5 are constituted of MOSFET's, and the operations of respective MOSFET's are controlled in accordance with the data signal DATA and reversed data signal XDATA so as to switch the electric current path of the circuit to thereby conduct the charge and discharge of the capacitor 4." (Inoue, Column 9, Lines 55-60) Figure 1 shows the switch 3 to drive the signal to LD 2. The output is connected to the light emitting element 2 and the gate is the controlling connection.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the MOSFET as taught by Inoue with Yamazaki's circuitry, as modified by the other teachings, with the motivation that the MOSFET "reduces the conventional unstable operation of the current source 1 due to charging and discharging of the capacitor **4**, thereby enabling the stable high speed modulation of the light emitting element **2**." (Inoue, Column 9, Lines 65-67)

Yamazaki teaches in Claim 10:

The display driver device as claimed in claim 9, wherein the driving transistor **(Figure 23, transistor 708)**

Yamazaki does not explicitly teach the driving transistor "being a field effect transistor, and the controlling connection is a gate of the field effect transistor."

However, in the same field of endeavor, displays for luminescent devices, Inoue teaches "the current switch 3 and boosting switch 5 are constituted of MOSFET's, and the operations of respective MOSFET's are controlled in accordance with the data signal DATA and reversed data signal XDATA so as to switch the electric current path of the circuit to thereby conduct the charge and discharge of the capacitor 4." (Inoue, Column 9, Lines 55-60) Figure 1 shows the switch 3 to drive the signal to LD 2. The output is connected to the light emitting element 2 and the gate is the controlling connection.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the MOSFET as taught by Inoue with Yamazaki's circuitry, as modified by the other teachings, with the motivation that the MOSFET "reduces the conventional unstable operation of the current source 1 due to charging and discharging of the capacitor **4**, thereby enabling the stable high speed modulation of the light emitting element **2**." (Inoue, Column 9, Lines 65-67)

Response to Arguments

5. Applicant's arguments considered, but are respectfully considered to not be persuasive.

Applicant argues that Yamazaki's 703 in Figure 23 is not a picture element, used for displaying the image to the user. However, the claim language does not explicitly claim a pixel, just a picture element, which is a broader variation. Yamazaki does indeed teach that 703 is indeed an electroluminescent element in [0408]-[0411], which is a picture element. He further teaches that the same levels are applied to both types of picture elements in Figure 23.

Applicant also argues against a driving transistor 708 of Yamazaki, but this also is respectfully not persuasive. Examiner does not see why 708 has to be interpreted as being part of 704 and why it cannot be considered a separate element, as nothing in the claim states this and it isn't a conflict with it being positively recited elsewhere in the claim language. Furthermore, the first and second current paths have been interpreted as the current paths connected to the negative and positive terminals of the transistor, respectively, with the first current path being connected to the output path of the amplifier. This actually mirrors Applicant's own Figure 5 in the examiner's opinion. Examiner does not understand Applicant's arguments on this part as the two paths are defined and satisfy the claim language.

Applicant is advised to claim the broad picture element language stronger and in a way that Figure 23 could not read on it to overcome the current rejection and for allowance of the case.

Conclusions

Applicant's amendments and non-persuasive arguments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

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Supervisory Patent Examiner, Art Unit 2629